REMARKS

II. Response to Office Action

A. Status of the Pending Application

Claims 25-32 and 34-50 are pending in the application. Claims 1-24 have been cancelled. Claims 25-28, 31-32, 34-37, 39, 41-44, 47, 49 and 50 stand rejected under 35 U.S.C. § 102(e) as unpatentable over *Hsu* (U.S. Patent No. 6,555,467). Claims 42 and 45 stand rejected under 35 U.S.C. § 102(e) as unpatentable over Grill (U.S. Patent No. 6,413,852). Claim 40 stands rejected under 35 U.S.C. § 103(a) as unpatentable over *Hsu* in view of Ibanbdeljalil (U.S. Patent No. 6,365,958). Claims 29 and 48 stand rejected under 35 U.S.C. § 103(a) as unpatentable over *Hsu* in view of Brown (U.S. Patent No. 6,030,896). Claim 6 stands rejected under 35 U.S.C. § 103(a) as unpatentable over *Hsu* in view of Ito (U.S. Patent No. 6,573,607). Claim 38 stands rejected under 35 U.S.C. § 103(a) as unpatentable over *Hsu* in view of Kohl (U.S. Patent Publication No. 2002/0081787).

B. Claim Rejections

1. Claims 25-28, 31-32, 34-37, 39, 41-44, 47, 49 and 50 are not anticipated by the Cited References.

1a. The *Hsu* Reference

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Amended Claim 25 recites, for example and without limitation, a semiconductor layer arrangement, comprising a substrate; a layer being arranged on the substrate, the layer including a first subregion and a second subregion arranged proximate to the first subregion, the first subregion being a decomposable material and the second subregion having a structure of nondecomposable material; a covering layer positioned on the layer; an electrically conductive passivation layer positioned between the structure of nondecomposable material and the covering layer; wherein the decomposable material is diffusible through the covering layer and wherein the structure is formed from copper and is at least partially sheathed by a passivation layer by means of a chemical vapor

deposition process. Amended claim 42 recites, for example and without limitation, a process for forming a layer arrangement, comprising forming a layer on a substrate, the layer including a first subregion and a second subregion arranged proximate to the first subregion, the first subregion having decomposable material and the second subregion having a structure of a nondecomposable material; forming a covering layer on the layer including the first subregion and second subregion; and forming an electrically conductive passivation layer at least between the structure and the covering layer; wherein the decomposable material is removable from the layer arrangement by diffusing through the covering layer and wherein the structure is formed from copper and is at least partially sheathed by a passivation layer by means of a chemical vapor deposition process. The Examiner asserts that *Hsu* (U.S. Patent No. 6,555,467) in combination with Ito (U.S. Patent No. 6,573,607) disclose all of the recitations of amended claims 25 and 42. Applicant respectfully disagrees.

Regarding the rejection as being anticipated by *Hsu*, the Examiner has argued in item 4 on page 2 of the Office action, that:

> *Hsu* teaches a semiconductor arrangement. Said arrangement comprises a substrate (12) (fig 1) (column 2 lines 20-30). A layer arranged on the substrate (12). The layer including a first subregion (18) and a second subregion (42, 72) arranged proximate the first subregion (18) (fig 7). The first subregion (18) being a decomposable material (column 2 lines 30-60) and the second subregion (42) having a structure of non-decomposable material (column 3 lines 10-40). A covering layer (62) positioned on the layer (column 4 lines 55-65). ***An electrically conductive passiviation layer (40, 70) positioned between the structure of the non-decomposable material and the covering layer (82) (fig 11)*** (column 4 lines 50-65). Wherein the decomposable material (18) is diffusible through the covering layer (82) (fig 11,12) (column 5 lines 1-5).

(Emphasis added.)

As can be seen from FIG. 12 of *Hsu*, the "barrier metal 40" and "barrier metal 70" is ***not*** positioned between the structure of non-decomposable material and the covering layer. (See also FIG. 7 and FIG. 10 of *Hsu*.). Col. 4, lines 48-62, of *Hsu* states:

Repeating the steps of depositing additional sacrificial layers, etch stops, and hard masks, followed by patterning and selective etching as described above can be used to form additional interconnect levels. As shown in FIG. 11, a total of three interconnect levels have been formed. Additional levels are also possible, by repeating

the process. Once the final interconnect level is completed, a ***capping layer 80 of silicon nitride or boron nitride*** is deposited to a thickness of approximately between 5 nm and 10 nm and patterned, preferably using photoresist, to protect the top copper layer. This capping layer is preferably slightly larger than the trench of the top metal lines, but it is not very dimensionally critical. Any remaining photoresist is then stripped. A passivation layer 82, preferably of oxide, is deposited to a thickness of between approximately 500 nm and 1500 nm.

In microelectronic technology, silicon nitride is usually formed using chemical vapor deposition (CVD) method, or one of its variants, such as plasma-enhanced chemical vapor deposition (PECVD). It is usually used either as an insulator layer to electrically isolate different structures or as an etch mask in bulk micromachining. Similarly, due to its excellent dielectric and insulating properties, BN [boron nitride] is used in electronics e.g. as a substrate for semiconductors, microwave-transparent windows, structural material for seals, electrodes and catalyst carriers in fuel cells and batteries. Hence, the "capping layer 80"in *Hsu* between the structure of non-decomposable material and the covering layer is an electrical ***insulator***. In contrast, in the present invention the passivation layer positioned between the structure of non-decomposable material and the covering layer is electrically ***conductive***.

Accordingly, *Hsu* does not disclose or suggest all of the recitations of amended claims 25 and 42. Applicant respectfully requests allowance of claims 25 and 42.

Claims 26-32 and 34-50 ultimately depend from claims 25 and 42. Accordingly, claims 26-32 and 34-50 are patentable for at least the reasons discussed above for claims 25 and 42. Applicant respectfully requests the Examiner to remove the rejections to claims 26-32 and 34-50 and allow the claims.

In addition, claim 37 recites an additional feature not present in the *Hsu*. Claim 37 depends from claim 36 and recites, *inter alia,* that the decomposable material comprises any one of polyester, polyether, polyethylene glycol, polypropylene glycol, polyethylene oxide, polypropylene oxide, polyacrylate,

polymethacrylate, polyacetal, polyketal, polycarbonate, polyurethane, polyether ketone, cycloaliphatic polymer, polynorbornene, aliphatic polyamide, Novolak, polyvinylphenol, an epoxy compound, copolymer of these compounds, terpolymer and combinations thereof. The Examiner asserts that *Hsu* discloses the recitations of claim 37. In particular, the Examiner asserts that *Hsu* discloses a thermally decomposable material composed of polynorbornene. (See Office Action mailed September 27, 2006, at 4). Applicant respectfully disagrees.

Hsu discloses the use of Unity sacrificial polymer, which is a copolymer of butylnorbornene and triethyloxysilyl norbornene (*Hsu*, Col. 2, ll. 35-41). However, butylnorbornene is not polynorbornene. Therefore, because *Hsu* does not disclose or suggest all of the recitations of claim 37, *Hsu* does not anticipate claim 37 under 35 U.S.C. § 102(e) as asserted by the Examiner. Applicant respectfully requests the Examiner to remove the rejection of claim 37.

Accordingly, Applicant requests the Examiner to remove the rejections of claims 25-32 and 34-50, and notice to that effect is earnestly solicited.

2a. Claims 42 and 45 are not anticipated by *Grill* (U.S. Patent No. 6,413, 852)

The Examiner has argued in item 43 on page 6 of the Office action, that:

> Grill teaches a method of making a semiconductor layer arrangement. Said arrangement comprises a providing substrate (100) (fig la) (column 4 lines 45-65). Forming a layer arranged on the substrate (100). The layer including a first subregion (220) and a second subregion (185) arranged proximate the first subregion (220) (fig 4a) (column 5 lines 30-50). The first subregion (220) being a decomposable material (column 6 lines 30-65) and the second subregion (185) having a structure of non-decomposable material (column 5 lines 30-60). Forming a covering layer positioned on the layer (fig 4b) (column 9 lines 5-30). ***Forming an electrically conductive passiviation layer (440, 450) positioned between the structure of the non-decomposable material and the covering layer*** (fig 4b) (column 9 lines 5-30). Wherein the decomposable material (220) is diffusible through the covering layer (fig 4b, 4c) (column 2 lines 20-40).

(Emphasis added.)

The references signs 440 and 450 are mentioned in *Grill* only in the paragraph in col. 9, lines 19-30.

> FIG. 4C shows how a selective, electroless metal (e.g., Co--P, Co--W--P, Co--Sn--P, Ni--P etc.) plating process is used to form ***protective coatings 440 and 450*** on the exposed surfaces of the conductive wiring and vias. In preferred embodiments, coating 450 would be introduced after the dielectric etch-back steps, i.e., performed on structures corresponding to FIGS. 1F and 1K, and coating 440 would be introduced after metal planarization, i.e., performed on structures corresponding to FIGS. 1I-1L. If desired, exposed regions of coating 440 might be passivated with a thin insulator.

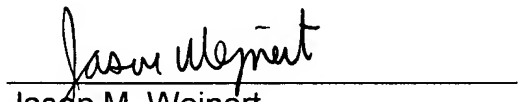
(Emphasis added.)

Consequently, there is no disclosure or suggestion in *Grill* that the "protective coatings 440 and 450" is an electrical ***conductor***. Neither *Hsu* nor *Grill* show (or suggests) the features of claims 25 and 42.

C. Summary

Pending Claims 25-32 and 34-50 are patentable. Applicant respectfully requests the Examiner grant early allowance of this application. The Examiner is invited to contact the undersigned attorney for the Applicant via telephone if such communication would expedite this application.

Respectfully submitted,



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